

**REMARKS**

Applicants respectfully make a Request for Continued Examination. Claims 1 and 3-15 are pending in the present application. Figures 1-4 and claims 1, 7 and 13 have been amended and claim 2 has been canceled by way of the present amendment. Applicant request that the present amendment be entered instead of the previously filed After Final Amendment in this application of October 16, 2006. Reconsideration is respectfully requested.

In the outstanding Office Action, Figures 1-3 have been indicated as needing a legend, such as Prior Art; claims 1-6 and 13-15 were rejected under 35 U.S.C. Section 103(a) as unpatentable over the Applicant's Prior Art Figure 2B (APAF) in view of U.S. Patent Publication No. 2002/0122280 (Ker et al. I); claims 7, 8 and 10-12 were rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of U.S. Patent No. 6,566,715 (Ker et al. II); and claim 9 was rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of Ker et al. II as applied to claim 7 above, and further in view of Ker et al. I.

***Drawing Objections***

Figures 1-3 were indicated to need a legend such as Prior Art. In response to the rejection, Figures 1-3 have been amended to include the legend "Background Art." Replacement sheets for Figures 1-3 including the legend "Background Art" are filed herewith. In addition, FIG. 4 has been amended to correct a drawing error. In particular, Patent Application Publication No. US 2005/0224882 A1 discloses at page 3, paragraph [0027], lines 6-7 states: "N-well 38 and N-well 37 are connected through contact 36, 30 to VDD." FIG. 4 has been amended to correctly illustrate this concept from the disclosure. Thus, Applicants respectfully submit that the amendments raise no question of new matter. As a result, Applicants request that the outstanding drawing objection be withdrawn.

***35 USC Section 103 Rejections***

Claims 1-6 and 13-15 were rejected under 35 U.S.C. Section 103(a) as unpatentable over APAF in view of Ker et al. I. Applicants respectfully traverse the rejection.

Claims 1, 7 and 13 have been amended to clarify the invention. In particular, claim 1 has been amended to recite:

wherein the first and third wells are *completely isolated from the drain, source and substrate contact, and*  
wherein the substrate contact is located outside the first, *second and third wells and directly connected to the substrate* (emphasis added).

Claims 7 and 13 have been amended in a similar manner. Support for the limitation is provided at least at page 3, paragraph [0027], lines 11-12; and shown at least in FIG. 4, references **28, 33, 34, 42, 44** and **50** of the published application (i.e., U.S. Patent Application Publication No. US 2005/0224882). Therefore, the amendments raise no questions of new matter.

The APAF discloses the implementation of an ESD NMOSFET in a triple well CMOS architecture.<sup>1</sup> In particular, the APAF discloses an additional N-Band **40** that constitutes an n-type doped region which in combination with the N-Wells **37** and **38** isolates the P-well **31** from the substrate **41**.<sup>2</sup> As can be seen from FIG. 2B of the specification, the triple well architecture of the background art is similar to the dual well architecture, *with the exception of the additional N-Band 40, and N-wells 37 and 38.*<sup>3</sup> N-wells **37** and **38** are connected in the embodiment shown to a source of positive potential VDD.<sup>4</sup> Additionally, two isolation regions **33** and **34** provide isolation for N-well **37** and N-well **38** from the substrate contact **30** and drain **26**, respectively.<sup>5</sup>

<sup>1</sup> *Id.* at page 2, paragraph [0024], lines 1-2.

<sup>2</sup> *Id.* at page 2, paragraph [0024], lines 2-5.

<sup>3</sup> *Id.* at page 2, paragraph [0024], lines 5-8.

<sup>4</sup> *Id.* at page 2, paragraph [0024], lines 8-10.

<sup>5</sup> *Id.* at page 2, paragraph [0024], lines 10-12.

However, the APAF nowhere discloses, as recited in independent claim 1:

*a path of substrate material extending through an opening in said conductive band region, increasing the substrate resistance in the path of the current which flows through said I/O pad to a substrate contact and drain during an ESD event and electrically connecting the second well to the substrate,*

*wherein the first and third wells are completely isolated from the drain, source and substrate contact, and wherein the substrate contact is located outside the first, second and third wells and directly connected to the substrate (emphasis added).*

That is, the APAF nowhere discloses: “the first and third wells are *completely isolated from the drain, source and substrate contact*” and “the substrate contact is located outside the first, second and third wells and directly connected to the substrate;” as recited in the presently amended claim 1 and as similarly recited in claims 7 and 13. Therefore, the APAF does not disclose the claimed invention.

In addition, the outstanding Office Action acknowledges deficiencies in the APAF and attempts to overcome these deficiencies by combining the APAF with Ker et al. I. However, Ker et al. I cannot overcome all of the deficiencies of the APAF as will be discussed below.

Ker et al. I discloses an electrostatic discharge (ESD) protection component with a deep-N-well structure in CMOS technology.<sup>6</sup> In particular, Ker et al. I discloses an N-type Silicon Controlled Rectifier (NSCR) device with a deep N-well, as shown in FIG. 5. Further, Ker et al. I discloses that there are three nodes in the NSCR structure: (1) the anode; (2) the cathode; and (3) the control gate (VGN).<sup>7</sup>

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<sup>6</sup> Ker et al. I at ABSTRACT.

<sup>7</sup> *Id.* at page 3, paragraph [0047], lines 2-4.

In addition, Ker et al. I discloses that the PNPN structure of the NSCR is composed of the P+ diffusion **52**, the N-well **42**, the P-well **40** and the N+ diffusion **46**.<sup>8</sup> The P+ diffusion **52** is used as the anode of the NSCR device and an NMOS is inserted into the P-well **40**.<sup>9</sup> The drain of the NMOS is formed by the N+ diffusion **44** at the P-N junction of the P-well **40** and the N-well **42**.<sup>10</sup> The source of the NMOS is formed by the N+diffusion **46**, used as the cathode of the NMOS device.<sup>11</sup>

Further, Ker et al. I discloses that in this modified device structure, the P-well **40** of the NSCR device is partially connected to the common P-substrate **30**.<sup>12</sup> But the two deep N-well regions **3201** and **3202** are placed closer to limit the connection region of the P-well **40** and the P-substrate **30**, thereby increasing the equivalent resistance between them.<sup>13</sup> The deep N-well **3201** is connected to N-well **60**, the deep N-well **3202** is connected to N-well **42**.<sup>14</sup> When proper voltage is applied to the control gate VGN, the trigger current from the NMOS into the P-well **40** turns on the NSCR more quickly within the limited connection region.<sup>15</sup> Moreover, Ker et al. I discloses that the P-substrate **30** is connected to VSS *through a P-well 36 to the P+ diffusion 54* (emphasis added).<sup>16</sup>

However, the Ker et al. I nowhere discloses, as recited in independent claim 1:

wherein the first and third wells are *completely isolated*  
*from the drain, source and substrate contact, and*  
*wherein the substrate contact is located outside the first, second*  
*and third wells and directly connected to the substrate* (emphasis  
added).

<sup>8</sup> *Id.* at page 3, paragraph [0047], lines 4-6.

<sup>9</sup> *Id.* at page 3, paragraph [0047], lines 6-8.

<sup>10</sup> *Id.* at page 3, paragraph [0047], lines 8-10.

<sup>11</sup> *Id.* at page 3, paragraph [0047], lines 10-11.

<sup>12</sup> *Id.* at page 3, paragraph [0047], lines 11-13.

<sup>13</sup> *Id.* at page 3, paragraph [0047], lines 14-17.

<sup>14</sup> *Id.* at page 3, paragraph [0047], lines 17-18.

<sup>15</sup> *Id.* at page 3, paragraph [0047], lines 14-21.

<sup>16</sup> *Id.* at page 3, paragraph [0044], lines 19-20.

That is, the Ker et al. I nowhere discloses: “the substrate contact is located outside the first, second and third wells and directly connected to the substrate;” as recited in the presently amended claim 1 and in similar language in claims 7 and 13. Therefore, the Ker et al. I does not overcome all of the deficiencies of the APAF.

In addition, it is noted that Ker et al. I discloses a substrate contact **54** that is connected to VSS.<sup>17</sup> In contrast, the APAF discloses a substrate contact **50** connected to VDD. That is, Ker et al. I teaches away from the disclosed structure and function of the APAF. Further, as discussed above, the APAF clearly does not include an opening in the N-Band **40**. Moreover, Ker et al. I nowhere discloses the structure recited in claim 1 of: “first, second and third wells formed in the substrate and separated by shallow well isolation regions.”

As indicated, the arguments made above for claims 1 are also applicable to claims 7 and 13. Thus, at least for the reasons discussed above, claims 7 and 13 are not disclosed by the APAF and Ker et al. I. Therefore, at least for the reasons above, it is respectfully submitted that neither the APAF nor Ker et al. I, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention and that claims 1, 5, 13 and 14, and claims dependent thereon, patentably distinguish thereover.

Claims 7, 8 and 10-12 were rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of Ker et al. II. Applicants respectfully traverse the rejection.

As indicated above, amended claim 7 includes similar language to that found in amended claim 1. That is, claim 7 recites:

providing a resistive path from said well to a substrate contact located outside of said *triple well and directly connected to a substrate*, whereby the trigger voltage of the said ESD NMOSFET is reduced due to said resistive path between said substrate contact and said I/O pad and

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<sup>17</sup> Ker et al. I at FIG. 4b.

wherein a first, second and third wells are formed in the substrate of the triple well CMOS structure, a first well and third well of the triple well CMOS structure are completely isolated from a drain and source of the ESD NMOSFET, and

*wherein the substrate contact is located outside the first, second and third wells and completely isolated from the drain and source of the ESD NMOSFET* (emphasis added).

Thus, at least for the reasons discussed above for claim 1, the APAF also does not disclose all of the limitations of claim 7.

The outstanding Office Action acknowledges deficiencies in the APAF and attempts to cure those deficiencies with Ker et al. II. However, Ker et al. II cannot overcome all of the deficiencies of the APAF as discussed below.

Ker et al. II discloses a substrate-triggered technique to effectively improve the ESD robustness of integrated circuit (IC) products.<sup>18</sup> In particular, Ker et al. II discloses a substrate-triggered NMOS is positioned in a p-well 32 on a p-substrate 30.<sup>19</sup> Two poly-silicon gates 34, serving as the gate (electrode) of the substrate-triggered NMOS, are positioned above the p-well 32.<sup>20</sup> Two n+ doped regions 36, functioning as the drain (electrode) of the substrate-triggered NMOS, are positioned between poly-silicon gates 34 on the surface of the p-well 32.<sup>21</sup> Between the n+ doped regions 36, a p+ doped region 40 is positioned for the electrical connection to p-well 32 and serves as the trigger node for the substrate-triggered NMOS.<sup>22</sup> Isolation object(s) 42, in this example, the silicon oxide formed by the shallow trench isolation processes, isolate the p+ doped region 40 from the n+ doped regions 36.<sup>23</sup> The two n+ doped regions 38 on the surface(s) of p-well(s) 32 provide the source (electrode) of the substrate-triggered NMOS.<sup>24</sup> As

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<sup>18</sup> Ker et al. II at ABSTRACT.

<sup>19</sup> *Id.* at column 1, lines 16-17.

<sup>20</sup> *Id.* at column 1, lines 17-20.

<sup>21</sup> *Id.* at column 1, lines 20-23.

<sup>22</sup> *Id.* at column 1, lines 23-25.

<sup>23</sup> *Id.* at column 1, lines 26-28.

<sup>24</sup> *Id.* at column 1, lines 28-31.

shown in FIG. 5B, one of the n+ doped regions 38, a p-well 32 and one of the n+ doped region 36 together can construct a parasitic npn bipolar junction transistor (BJT).<sup>25</sup>

In addition, Ker et al. II discloses an n-well 44 is positioned to partially overlay and electrically couple with the n+ doped region 38.<sup>26</sup> Beside the n+ doped region 38, a p+ doped region 46 forms the electrical connection to p-well 32'.<sup>27</sup> All the surfaces of the p+ regions 46 and 40 are capped by silicide material.<sup>28</sup> The areas of the n+ doped regions 36 and 38 are patterned by a photo mask 52 to block silicide material on their surfaces but the contact areas will be still covered with silicide.<sup>29</sup>

Further, Ker et al. II discloses the contacts 54 for the n+ doped regions 36 must be separated from poly-silicon gate 34 by a specific distance, as shown in FIG. 5A, to sustain a higher ESD stress.<sup>30</sup> The shortest conductive path from the base of the npn BJT to the p+ doped region 46 must travel around n-well 44, to take advantage of the higher resistance provided by spread resistor Rsub.<sup>31</sup>

However, it is respectfully submitted that Ker et al. II cannot overcome all of the deficiencies of the APAF regarding claim 7. In particular, Ker et al. II nowhere discloses, as claim 7 recites:

providing a resistive path from said well to a substrate contact located outside of said *triple well and directly connected to a substrate*, whereby the trigger voltage of the said ESD NMOSFET is reduced due to said resistive path between said substrate contact and said I/O pad and  
wherein a first, second and third wells are formed in the substrate of the triple well CMOS structure, a first well and third

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<sup>25</sup> *Id.* at column 1, lines 31-34.

<sup>26</sup> *Id.* at column 1, lines 35-36.

<sup>27</sup> *Id.* at column 1, lines 36-37.

<sup>28</sup> *Id.* at column 1, lines 37-39.

<sup>29</sup> *Id.* at column 1, lines 39-42.

<sup>30</sup> *Id.* at column 1, lines 43-45.

<sup>31</sup> *Id.* at column 1, lines 45-49.

well of the triple well CMOS structure are completely isolated from a drain and source of the ESD NMOSFET, and

*wherein the substrate contact is located outside the first, second and third wells and completely isolated from the drain and source of the ESD NMOSFET (emphasis added).*

That is, at least for the same reasons discussed above for claim 1, Ker et al. II cannot overcome the deficiencies of the APAF.

Further, it is respectfully submitted that Ker et al. II teaches away from the claimed invention. In particular, Ker et al. II discloses “an n-well is positioned to partially overlay and electrically couple with the n+ doped region 38” and that “n+ doped regions 38 on the surface(s) of p-well(s) 32 provide the source (electrode).”<sup>32</sup>

Therefore, at least for the reasons above, it is respectfully submitted that neither the APAF nor Ker et al. II, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention and that claim 7, and claims dependent thereon, patentably distinguish thereover.

Claim 9 was rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of Ker et al. II as applied to claim 7 above, and further in view of Ker et al. I. Applicants respectfully traverse the rejection.

Claim 9 is dependent on claim 7. Thus, at least for the reasons discussed above for claim 7, the APAF and Ker et al. II do not disclose all of the limitations of claim 9. In addition, the outstanding Office Action acknowledges deficiencies in the APAF and Ker et al. II and attempts to cure those deficiencies with Ker et al. I. However, as discussed above, Ker et al. I cannot overcome all of the deficiencies of the APAF and Ker et al. II. In particular, Ker et al. I nowhere discloses, as claim 7 recites:

providing a resistive path from said well to a substrate contact located outside of said *triple well and directly connected to a substrate*, whereby the trigger voltage of the said ESD

<sup>32</sup> See Ker et al. II at column 4, lines 30-33 and 35-38.

NMOSFET is reduced due to said resistive path between said substrate contact and said I/O pad and

wherein a first, second and third wells are formed in the substrate of the triple well CMOS structure, a first well and third well of the triple well CMOS structure are completely isolated from a drain and source of the ESD NMOSFET, and

*wherein the substrate contact is located outside the first, second and third wells and completely isolated from the drain and source of the ESD NMOSFET (emphasis added).*

That is, at least for the same reasons discussed above for claim 1 and claim 7, Ker et al. I cannot overcome the deficiencies of the APAF and Ker et al. II.

Therefore, at least for the reasons above, it is respectfully submitted that none of the APAF, Ker et al. I, and Ker et al. II, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention, and that claim 9, and claims dependent thereon patentably distinguish thereover.

***Conclusion***

Based on the above amendments and arguments, Applicant respectfully submits that the application is in condition for allowance. If a fee is due, please charge Deposit Account No. 50-3223, under Order No. 21806-00158-US, from which the undersigned is authorized to draw.

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